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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/930,956	08/17/2001	Jun Koyama	12732-071001	1626

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EXAMINER	
SHENG, TOM V	

ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 05/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/930,956	KOYAMA ET AL.	
	Examiner	Art Unit	
	Tom V Sheng	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-62* is/are pending in the application.

4a) Of the above claim(s) *54-61* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-53 and 62* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/16/05, 3/1/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 23-35 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 21-32 of copending Application No. 09/931061, hereinafter case 061. Although the conflicting claims are not identical, they are not patentably distinct from each other because even though claims 23-35 of the current application are directed to liquid crystal display and claims 21-32 of the copending application are directed to electro-luminescent display,

the underlying pixel-memory structure (i.e. the nxm memory circuits, nxk non-volatile memory circuits, 2n memory circuit selecting units, 2n non-volatile memory circuit selecting unit) and

pixel-memory writing/reading structure (the source signal line, n writing gate signal lines, n reading gate signal lines, n writing transistors, n reading transistors,

connections from each gate electrode of the n writing transistors to one of the n writing gate signal lines, from each input electrode of the n writing transistors to the source signal line, from each output electrode of the n writing transistors to one of the m circuits out of the nxm memory circuits, from each output electrode of the n writing transistors to one of the k circuits out of the nxk non-volatile memory circuits, from each gate electrode of the n reading transistors to one of the n reading gate signal lines, from each input electrode of the n reading transistors to one of the m circuits out of the nxm memory circuits, from each input electrode of the n reading transistors to one of the k circuits out of the nxk non-volatile memory circuits,) are similarly claimed between the two claims. Claim 21 of case 061 differs from claim 23 of the current application in that claim 21 recites the pixel element comprising EL element and a corresponding EL drive transistor while claim 23 recites the pixel element as a liquid crystal element.

It would have been obvious for one of ordinary skill in the art at the time the invention was made that the pixel-memory structure and functionality are factually independent from the display type.

Claims 36-49 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 33-45 of copending Application No. 09/931061, hereinafter case 061. Although the conflicting claims are not identical, they are not patentably distinct from each other because even though claims 36-49 of the current application are directed to liquid crystal display and claims 33-45 of the copending application are directed to electro-luminescent display, just as analyzed above with regard to claims 23-35, the underlying pixel-memory

structure and pixel-memory writing/reading structure are similarly claimed. It would have been obvious for one of ordinary skill in the art at the time the invention was made that the pixel-memory structure and functionality are factually independent from the display type.

Claims 50-53 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 46-48 of copending Application No. 09/931061, hereinafter case 061. Although the conflicting claims are not identical, they are not patentably distinct from each other because the method of driving the electronic device for read and write operations are actually equivalent. It would have been obvious for one of ordinary skill in the art at the time the invention was made that the driving method is applicable to either LCD or EL type of displays and the electronic device incorporating the display can be any of the common products as claimed.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 62 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura et al. (US 5,945,972) in view of Kobayashi et al. (US 4,432,610).

As for claim 62, Okumura teaches a liquid crystal display device (fig. 6-9) having a pixel having:

a liquid crystal element (liquid crystal cell 276); and

a plurality of sub-pixels (a color pixel is common in the art made of 3 primary color sub-pixels), each of the plurality of sub-pixels comprising:

a memory circuit (fig. 8 or 9; first memory 230a or 230a');

another memory circuit (second memory 230b or 230b' but is not non-volatile);

a first switch (first transfer gate 232a) electrically connected to the memory circuit (as shown);

a second switch (second transfer gate 233a) electrically connected to the first switch and to the another memory circuit (as shown);

a third switch (third transfer gate 233b) electrically connected to the liquid crystal element (cell 276) and to the memory circuit (as shown); and

a fourth switch (fourth transfer gate 232b) electrically connected to the liquid crystal element (cell 276) and to the another memory circuit (as shown). See column 17, line 56 through column 18, line 41.

Okumura's memory circuits (230a, 230b, 230a', 230b') are either DRAM or SRAM, which are both volatile type of memory. Thus, Okumura does not teach the another memory circuit as a **non-volatile memory circuit**.

Kobayashi teaches in the same field of liquid crystal display whereas each pixel also has an associated memory (memory cell 12-ij of LSI circuit array 12; fig. 2). Kobayashi further teaches the problem of memory erasure in the case of a momentary power failure (column 4, lines 57-61). To solve this problem, he teaches using modified LSI circuit array comprising nonvolatile memory transistors, so that the data stored would not be erased even in the case of a momentary power failure. See column 4, line 62 through column 5, line 12. At the time of the invention, one of ordinary skill in the art would, in view of Kobayashi's teaching, modify at least the another memory circuit as a non-volatile memory circuit for power failure protection. Moreover, the sub-pixel could be modified such that in the case of a power failure, the last image frame would go to the non-volatile memory circuit such that upon power recovery, the last image frame would still be available for display.

Therefore, it would have been obvious for one of ordinary skill in the art at the time the invention was made to modify Kobayashi's another memory circuit as non-volatile type to protect against power failure.

5. Claims 1, 4, 9-12, 15 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura and Kobayashi as applied to claim 62 above, and further in view of Perner (US 6,246,386 B1).

As for claim 1, as analyzed in claim 62, Okumura as modified by Kobayashi teaches a liquid crystal display having the memory circuit, non-volatile memory circuit, first switch, second switch, third switch and fourth switch, with the liquid crystal element

connected to the third and fourth switches. However, Okumura as modified does not teach the further limitations of having multiple sets of the memory circuit, non-volatile memory circuit, first switch, second switch, third switch and fourth switch, connected to drive a single liquid crystal element, as recited.

Perner further teaches, in the teaching of pixel memory for a liquid crystal display, incorporating an array of DRAM cells in each pixel according to the number of bits of data of a frame (column 5, lines 47-53). In particular, he teaches using 18 bits per pixel with 6 bits of grayscale for each color (i.e. color sub-pixel). At the time of the invention, one of ordinary skill in the art, would, based on the teaching of Perner, further incorporate multiples of Okumura/Kobayashi's memory circuit structure, so as to provide a broader grayscale resolution. That is, in the case 6 bits for each color, there would be 6 sets of the memories and switches as recited in claim 62.

Therefore, it would have been obvious for one of ordinary skill in the art at the time the invention was made to provide multiples of Okumura/Kobayashi's memory circuit structures because of the benefit of broader grayscale display.

As for claim 12, as analyzed in claim 1, Okumura as modified by Kobayashi and Perner teaches a liquid crystal display having multiple sets of memory circuit, non-volatile memory circuit, first switch, second switch, third switch and fourth switch, with the liquid crystal element connected to the third and fourth switches, thus providing a broader grayscale display. However, Okumura as modified does not teach the further limitations of having m memory circuits (corresponding to m frames) and k non-volatile memory circuits (corresponding to k frames).

It would have been obvious for one of ordinary skill in the art at the time the invention was made; however, that the provision of multiple frames are well known in the art as a way of freeing up a graphics processor for other tasks. With this, the graphics processor only needs to send display data when the data within the memory drops to a threshold, such as 1 frame of data or no data.

As for claims 4 and 15, Perner's memory circuits are DRAM cells.

As for claims 9 and 20, Kobayashi teaches the forming of non-volatile memory transistors on a monocrystalline silicon substrate.

As for claims 10-11 and 21-22, LCD devices are well known to be incorporated in an electronic device such as television set, personal computer, portable terminal, video camera, and head mounted display.

6. Claims 2, 5, 13, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perner and Kobayashi and Okumura as applied to claims 1 and 12 above, and further in view of Yamazaki et al. (US Patent 5699078).

As for claims 2, 5, 13, and 16, Perner teaches the use of DRAM for the memory circuits. Perner does not teach using SRAM for the memory circuits and EEPROM for the non-volatile memory circuits.

Yamazaki teaches the incorporation of a memory in which information on the characteristics of the pixels are stored, into a liquid crystal device. See column 2, lines 23-30. Moreover, Yamazaki teaches that volatile memories such as DRAM and SRAM,

as well as non-volatile memories such as EEPROM and flash memories are suitable choices. See column 4, lines 36-40.

It would have been obvious for one of ordinary skill in the art at the time the invention was made to incorporate SRAM of Yamazaki as the memory circuits and EEPROM of Yamazaki as the non-volatile memory circuits because they are all suitable choices in implementing the memories. Certainly, factors such as design complexity, sizes, and etc. would come into play.

7. Claims 3 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perner and Kobayashi and Okumura as applied to claims 1 and 12 above, and further in view of Yamazaki et al. (US Patent 5349366).

As for claims 3 and 14, Perner teaches the use of DRAM for the memory circuits. Perner does not teach using FeRAM for the memory circuits.

Yamazaki teaches the incorporation of material such as ferroelectrics to function as memory.

It would have been obvious for one of ordinary skill in the art at the time the invention was made that the memory taught by Yamazaki can be applied for the memory circuits of Perner, because it would allow rewriting only specified pixels as taught by Yamazaki and would also simply constitute an alternative choice of memory component in the pixel. See Abstract and column 9, lines 40-55.

8. Claims 6 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perner and Kobayashi and Okumura as applied to claims 1 and 12 above, and further in view of Parks (US Patent 5471225).

As for claims 6 and 17, Perner teaches a LCD device incorporating an array of memory circuits with each pixel. However, Perner does not teach that the memory circuits are formed on a glass substrate.

Parks teaches a LCD having a plurality of storage cells. Further, provided across a glass material are the storage cells comprising bit lines, word lines, display electrodes, pass-gate transistors, and latching circuits for storing video data.

It would have been obvious for one of ordinary skill in the art at the time the invention was made that glass substrate of Parks is a good insulator for laying the memory and driving circuits of an LCD display. Also, the transparent property of glass lends naturally to use with liquid crystal display, and thus accounts for the common usage.

9. Claims 7 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perner and Kobayashi and Okumura as modified by Parks as applied to claims 1/12 and 6/17 above, and further in view of Fonash et al. (US Patent 5945866).

As or claims 7 and 18, Perner as modified teaches a LCD device having an array of memory circuits per pixel; wherein the memory circuits are formed on a glass substrate.

Perner as modified does not teach that a plastic substrate can be used also.

Fonash teaches that TFTs can be deposited on either glass or plastic substrate (figure 1). TFTs are transistor circuits used for driving as well as memory circuits of Perner as modified. See column 1, lines 44-52.

It would have been obvious for one of ordinary skill in the art at the time the invention was made that either substrate, glass or plastic of Fonash, can be used for manufacturing the circuits, which is readily recognized as an alternative material choice.

10. Claims 8 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perner and Kobayashi and Okumura as modified by Parks as applied to claims 1/12 and 6/17 above, and further in view of Johnson (US Patent 4752118).

As or claims 8 and 19, Perner as modified teaches a LCD device having an array of memory circuits per pixel; wherein the memory circuits are formed on a glass substrate.

Perner as modified does not teach that a stainless steel substrate can be used also.

Johnson teaches that amorphous integrated circuits can be deposited on either glass or stainless steel (column 1, line 22 - column 2, line 2). In the case of stainless steel, it should first be coated with a layer of insulating layer (column 8, line 61 - column 9, line 2).

It would have been obvious for one of ordinary skill in the art at the time the invention was made that either substrate, glass or stainless steel of Johnson, can be

used for manufacturing the circuits, which is readily recognized as an alternative material choice.

Response to Arguments

11. Applicant's arguments with respect to claims 1, 4, 9-12, 15, 20-22 and 62 have been considered but are moot in view of the new ground(s) of rejection.

Comment

Addition of qualifier "volatile" to memory circuits in order to clearly differentiate from the non-volatile memory circuits in the claims is recommended.

The Examiner has mistakenly conveyed allowance on claims 23-53 in the previous action. This is not proper in view of the ongoing double patenting rejection. Subsequently, allowance on claims 23-53 is withdrawn with sincere apology. This is non-final rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tom V Sheng whose telephone number is (571) 272-7684. The examiner can normally be reached on 9:00am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tom Sheng
April 22, 2005

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